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USPT	((8 or eight) adj1 bit)	57394	L1

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1. Document ID: US 5025414 A

L37: Entry 1 of 1 File: USPT Jun 18, 1991

DOCUMENT-IDENTIFIER: US 5025414 A
TITLE: Serial bus interface capable of transferring data in different formats

ABPL:
A serial bus interface includes a shift register for receiving and transmitting serial data, a first selector coupled to a serial input of the shift register selectively coupling the serial input of the shift register to either of two serial data lines, and a second selector coupled to a serial output of the shift register selectively coupling the serial output of the shift register to one of the two serial data lines. A clock generator, capable of generating a clock pulse in two different formats, is coupled to a clock line. The clock generator operates to output to the clock line a clock pulse in accordance with a format utilized by one of the serial data lines.

BSPR:
The above and other objects of the present invention are achieved in accordance with the present invention by a serial bus interface comprising a shift register receiving and transmitting serial data, a first selector coupled to a serial input of the shift register selectively coupling the input of the shift register to one of at least two serial data lines, a second selector coupled to a serial output of the shift register selectively coupling the output of the shift register to one of the serial data lines, and a clock generator coupled to a clock line and capable of generating a clock pulse in at least two different formats, the clock generator operating to output to the clock line a clock pulse in accordance with a format adopted in one of the serial data lines selected by a selector.

DEPR:
Now, operation will be explained using a first example in which 8-bit data is transferred from the microcomputer 10 to the slave IC 34 and using a second example in which the microcomputer 10 receives 9-bit data from the slave IC 36.

DEPR:
In this condition, 8-bit parallel data to be transferred is written into the shift register 12 through the data buffer 38 from the internal bus 40. A transfer rate data is written into the clock selector 52 so that the selector 52 produces a clock signal of a designated pulse rate from the output of the clock oscillator 70. The clock control flag 48 is set to "1" as shown in FIG. 3. Further, a signal is supplied to a clear input CL of the counter 78 so as to clear the counter 78, and to the set input S of the flipflop 80 so that the Q output of the flipflop 80 is set to "1".

DEPR:
As mentioned above, since the counter 78 has three bits, when the counter 78 counts eight clock pulses, the counter 78 generates a carry signal as the interrupt signal, as shown in FIG. 3. This interrupt signal is supplied to the reset input of the flipflop 80 so that the Q output of the flipflop 80 is brought into "0". As a result, the NAND gate 72 is closed, and, the output of the clock pulse is stopped. The interrupt signal is also supplied to the CPU 42. In response to this signal, the CPU 42 reads the content of the selection flag 44, and discriminates the destination of the data communication. In this case, since the selection flag 44 is set with "1" indicating the data line 18 through which serial data is transferred in an 8-bit format, the CPU 42 can start preparation

serial data is transferred in an 8-bit format, the CPU 42 can start preparation for another data transfer or reception, or can restart suspended data processing if data communication is not necessary.

DEPR:
When receiving 8-bit data from the slave IC 34, since the selection flag 44 is set to "1", when the interrupt request signal is generated by the counter 78, the CPU judges from the content of the selection flag 44 that the destination of the data communication is the slave IC 34. In this case, the CPU 42 will not write "0" and "1" to the clock control flag 48.

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